AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (canceled).

2. (currently amended): A pulse width modulating device ~~according to claim 1, further~~ comprising:

a clock generating device which generates a first clock signal;

an operation device which operates the first clock signal and generates at least one processing clock signal whose phase is different than a phase of the first clock signal;

a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by said operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by said operation device; and

a counter which, after the pulse of the pulse width modulating signal is made to rise, counts a number of pulses of the remaining one of the first clock signal and the processing clock signal generated by said operation device,

wherein after said counter has counted a predetermined number of pulses, said pulse width modulating signal output device makes the pulse fall synchronously with the remaining one of the first clock signal and the processing clock signal generated by said operation device.

3. (currently amended): A pulse width modulating device ~~according to claim 1,~~ comprising:

a clock generating device which generates a first clock signal;

an operation device which operates the first clock signal and generates at least one processing clock signal whose phase is different than a phase of the first clock signal; and

a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by said operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by said operation device;

wherein said operation device is a delay device which delays the first clock signal by a predetermined period of time and generates a second clock signal which is delayed by the predetermined period of time.

4. (currently amended): A pulse width modulating device ~~according to claim 1,~~ comprising:

a clock generating device which generates a first clock signal;

an operation device which operates the first clock signal and generates at least one processing clock signal whose phase is different than a phase of the first clock signal; and

a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by said operation device, and makes the pulse of the pulse width modulating

signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by said operation device;

wherein said operation device is a plurality of delay devices which delay the first clock signal by respectively different predetermined periods of time, and generate a plurality of delay clock signals which are delayed by the respectively different predetermined periods of time.

5. (currently amended): A pulse width modulating device ~~according to claim 1,~~ comprising:

a clock generating device which generates a first clock signal;

an operation device which operates the first clock signal and generates at least one processing clock signal whose phase is different than a phase of the first clock signal; and

a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by said operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by said operation device;

wherein the first clock signal generated by said clock generating device has a rectangular waveform, and said operation device is an inverting device which inverts the first clock signal and generates a second clock signal.

6. (original): A pulse width modulating device according to claim 5, wherein said operation device is a delay device which delays the second clock signal by a predetermined period of time and generates a third clock signal delayed by the predetermined period of time.

7. (original): An exposure device comprising:

(a) a pulse width modulating device including:

(i) a clock generating device which generates a first clock signal;

(ii) an operation device which operates the first clock signal and generates at least one processing clock signal whose phase is different than a phase of the first clock signal; and

(iii) a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by said operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by said operation device; and

(b) a light source for exposure which emits light in accordance with a pulse width of respective pulses of the pulse width modulating signal outputted by said pulse width modulating signal outputting device provided at said pulse width modulating device.

8. (original): An exposure device according to claim 7, wherein said operation device is a delay device which delays the first clock signal by a predetermined period of time and generates a second clock signal which is delayed by the predetermined period of time.

9. (original): An exposure device according to claim 7, wherein said operation device is a plurality of delay devices which delay the first clock signal by respectively different predetermined periods of time, and generate a plurality of delay clock signals which are delayed by the respectively different predetermined periods of time.

10. (original): An exposure device according to claim 7, wherein the first clock signal generated by said clock generating device has a rectangular waveform, and said operation device is an inverting device which inverts the first clock signal and generates a second clock signal.

11. (canceled).

12. (currently amended): A pulse width modulating method ~~according to claim 11, further~~ comprising ~~the step of~~:

(a) generating a first clock signal;

(b) operating the first clock signal and generating at least one clock signal whose phase is different than a phase of the first clock signal;

(c) making a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the clock signal generated in step (b), and making the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the clock signal generated in step (b); and

(d) in step (c), after the pulse is made to rise, counting a number of pulses of the remaining one of the first clock signal and the clock signal generated in step (b),

wherein in step (c), after a predetermined number of pulses have been counted by step (d), the pulse is made to fall synchronously with the remaining one of the first clock signal and the clock signal generated in step (b).

13. (currently amended): A pulse width modulating method ~~according to claim 11,~~ comprising:

(a) generating a first clock signal;

(b) operating the first clock signal and generating at least one clock signal whose phase is different than a phase of the first clock signal; and

(c) making a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the clock signal generated in step (b), and making the pulse of the pulse

width modulating signal fall synchronously with a remaining one of the first clock signal and the clock signal generated in step (b);

wherein in step (b), the first clock signal is delayed by a predetermined period of time, and a second clock signal which is delayed by the predetermined period of time is generated.

14. (currently amended): A pulse width modulating method ~~according to claim 11,~~ comprising:

(a) generating a first clock signal;

(b) operating the first clock signal and generating at least one clock signal whose phase is different than a phase of the first clock signal; and

(c) making a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the clock signal generated in step (b), and making the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the clock signal generated in step (b);

wherein in step (b), the first clock signal is delayed by a plurality of respectively different predetermined periods of time, and a plurality of delay clock signals which are delayed by the plurality of respectively different predetermined periods of time are generated.

15. (currently amended): A pulse width modulating method ~~according to claim 11,~~ comprising:

(a) generating a first clock signal;

(b) operating the first clock signal and generating at least one clock signal whose phase is different than a phase of the first clock signal; and

(c) making a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the clock signal generated in step (b), and making the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the clock signal generated in step (b);

wherein the first clock signal generated in step (a) has a rectangular waveform, and in step (b), the first clock signal is inverted and a second clock signal is generated.

16. (original): A pulse width modulating method according to claim 15, further comprising the step of:

in step (b), delaying the second clock signal by a predetermined period of time and generating a third clock signal which is delayed by the predetermined period of time.

17. (original): An exposure method comprising the steps of:

(a) generating a first clock signal;

(b) operating the first clock signal and generating at least one clock signal whose phase is different than a phase of the first clock signal;

(c) making a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the clock signal generated in step (b), and making the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the clock signal generated in step (b); and

(d) emitting light so as to effect exposure in accordance with a pulse width of respective pulses of the pulse width modulating signal.

18. (original): An exposure method according to claim 17, wherein in step (b), the first clock signal is delayed by a predetermined period of time and a second clock signal which is delayed by the predetermined period of time is generated.

19. (original): An exposure method according to claim 17, wherein in step (b), the first clock signal is delayed by respectively different predetermined periods of time, and a plurality of delay clock signals which are delayed by the respectively different predetermined periods of time are generated.

20. (original): An exposure method according to claim 17, wherein the first clock signal generated in step (a) has a rectangular waveform, and in step (b), the first clock signal is inverted, and a second clock signal is generated.

21. (currently amended): A pulse width modulating device ~~according to claim 1, further~~ comprising:

a clock generating device which generates a first clock signal;

an operation device which operates the first clock signal and generates at least one processing clock signal whose phase is different than a phase of the first clock signal;

a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by said operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by said operation device; and

a selector which selects and outputs to the pulse width modulating signal output device one of the first clock signal and the processing clock signal, based on a clock selection signal input to the selector.

22. (currently amended): A pulse width modulating device ~~according to claim 1,~~ comprising:

a clock generating device which generates a first clock signal;

an operation device which operates the first clock signal and generates at least one processing clock signal whose phase is different than a phase of the first clock signal; and

a pulse width modulating signal output device which makes a pulse of a pulse width modulating signal rise synchronously with one of the first clock signal and the processing clock signal generated by said operation device, and makes the pulse of the pulse width modulating signal fall synchronously with a remaining one of the first clock signal and the processing clock signal generated by said operation device;

wherein the pulse width modulating signal output device comprises an R-S flip-flop.

23. (previously presented): An exposure device according to claim 7, the pulse width modulating device further including:

a selector which selects and outputs to the pulse width modulating signal output device one of the first clock signal and the processing clock signal, based on a clock selection signal input to the selector.

24. (previously presented): An exposure device according to claim 7, wherein the pulse width modulating signal output device comprises an R-S flip-flop.